package circuit 460 formed on the bottom of the capacitor. The packages have at least one conductive layer 440 and dielectric layers. The conductive layers are coupled using vias [440] 404. These vias can be formed using a laser and plating the opening created with the laser. Other techniques can be used to fabricate and connect the package layers. The embodiment of Figure 9, therefore, illustrates that the capacitor can be embedded in a multi-layer circuit package.

IN THE DRAWINGS

The drawings were objected to as failing to comply with 37 CFR 1.84(p)(5) because they include reference signs 200 and 420 not mentioned in the description. Further, it was observed in the Office Action that element "410" was designated as "vias" and not "a capacitor". Finally, the drawings were objected to as failing to comply with 37 CFR 1.84(p)(4) because the reference character "440" was used to designate both vias and a conductive layer.

The Applicant appreciates the thorough review and observations of the Examiner in this regard. Appropriate changes have been made to the text of the application by way of amendment. Proposed redline corrections made to Figures 5, 8, and 9 are submitted herewith in accordance with the recommendation of the Examiner. Such changes are made to maintain consistency and clarity within the application text, and no new matter has been added.

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect amendment of previously pending claims 1, 4-6, 9-14, and 17-21. Thus, claims 1-21 are currently pending in this application. Specific amendments to individual claims are detailed in the following marked up set of claims.

1. (Once Amended) A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over the substrate;

a first insulator layer located over the first conductive layer;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductor layer; and

a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical [interconnect] interconnection to the first, second and third conductor layers.

4. (Once Amended) The multi layer integrated circuit capacitor of claim 1 wherein at least one of the [conductor] conductive layers comprise a metal material and at least one of the insulator layers comprise $BaSrTiO_3$.

5. (Once Amended) The multi layer integrated circuit capacitor of claim 4 wherein at least one of the [conductor] conductive layers are fabricated from a copper.

6. (Once Amended) The multi layer integrated circuit capacitor of claim 1 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer [is] being patterned to form interconnect lines that selectively connect the plurality of [plurality of] conductive vias.

9. (Once Amended) A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over the substrate;

a first insulator layer located over the first conductive layer;

a second conductive layer located over the first insulator layer, the second conductive layer [is] being fabricated as a plurality of laterally spaced strips such that a surface area of the second conductive layer is less than a surface area of the first conductive layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer, the third conductive layer [is] being fabricated as a plurality of laterally spaced strips such that a surface area of the third conductive layer is less than the surface area of the second conductive layer;

a third insulator layer located over the third conductive layer;

a first plurality of conductive vias downwardly extending through the third insulator layer

to provide electrical [interconnect] interconnection to the third conductive layer;

a second plurality of conductive vias downwardly extending through the third insulator layer to provide electrical [interconnect] interconnection to the second conductive layer; and

a third plurality of conductive vias downwardly extending through the third insulator layer to provide electrical [interconnect] interconnection to the first conductive layer.

10. (Once Amended) The multi layer integrated circuit capacitor of claim 9 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer [is] being patterned to form interconnect lines that selectively connect at least one of the [plurality of plurality] pluralities of conductive vias.

11. (Once Amended) A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over the substrate;

a first insulator layer located over the first conductive layer;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductive layer;

a first plurality of conductive vias downwardly extending through the third insulator layer, the third conductive layer, the second insulator layer, the second conductive layer and the first insulator layer to provide electrical [interconnect] interconnection to the first and third conductive layers; and

a second plurality of conductive vias downwardly extending through the third insulator layer, the third conductive layer, and the second insulator layer to provide electrical [interconnect] interconnection to the second conductive layer.

12. (Once Amended) The multi layer integrated circuit capacitor of claim 11 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer [is] being patterned to form interconnect lines that selectively connect at least one of the

[plurality of plurality] pluralities of conductive vias.

13. (Once Amended) The multi layer integrated circuit capacitor of claim 11 wherein at least one of the conductive layers comprise a metal material and wherein at least one of the insulator layers comprise $BaSrTiO_3$.

14. (Once Amended) A circuit [package] board assembly comprising:

a [package] circuit board having a pair of supply voltage interconnect lines;

a first integrated circuit die mounted on the circuit board and electrically connected to the supply voltage interconnect lines; and

a second integrated circuit die mounted on the circuit board and electrically connected to the supply voltage interconnect lines, the second integrated circuit package [comprises] comprising a capacitor having:

a substrate;

a first conductive layer located over the substrate;

a first insulator layer located over the first conductive layer;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductive layer; and

a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical [interconnect] interconnection to the first, second and third conductive layers.

17. (Once Amended) The circuit board assembly of claim 14 wherein at least one of the conductive layers comprise a metal material and wherein at least one of the insulator layers comprise $BaSrTiO_3$.

18. (Once Amended) The circuit board assembly of claim 14 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer [is] being

patterned to form interconnect lines that selectively connect the plurality of plurality of conductive vias.

19. (Once Amended) A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over the substrate;

a first insulator layer located over the first conductive layer;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductive layer; and

a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical [interconnect] interconnection to the first, second, and third conductive layers, the plurality of conductive vias further [extend] extending through the substrate to provide electrical [interconnects] interconnection [on] to both a top surface and a bottom surface of the integrated circuit capacitor.

20. (Once Amended) The multi layer integrated circuit capacitor of claim 19 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer [is] being patterned to form interconnect lines that selectively connect the [plurality of] plurality of conductive vias.

21. (Once Amended) The multi layer integrated circuit capacitor of claim 1 wherein each of the conductor layers comprise a metal material and wherein each of the insulator layers comprise $BaSrTiO_3$.

REMARKS

Rejections Under 35 U.S.C.§112

Claims 6, and 14-18 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which